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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/706,813	11/12/2003	Gareth D. Edwards	X-1337 US	6961

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
ALPHONSE, FRITZ	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/706,813	Applicant(s) EDWARDS, GARETH D.
	Examiner Fritz Alphonse	Art Unit 2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Williams (U.S. Pat. No. 5,881,271) in view of Byers (US Pub. No. 2004/0243874).

As to claim 10, Williams (figs. 1-2) shows a clock management system including a clock input terminal configured to receive an input clock signal (270) having a first set of edges and second set of edges (col. 5, lines 38-55); a data input terminal (150) configured to receive a first set of data values associated with the first set of edges of the input clock signal and a second set of data values associated with the second set of edges of the input clock signal (col. 4, lines 18-27). Williams (fig. 1) shows a first register (241) coupled to the first clock terminal (270), wherein the first register is configured to latch the first set of data values in response to the third set of edges of the first clock signal; and a second register (236) coupled to the second clock terminal and the data input terminal, wherein the second register is configured to latch the second set of data values in response to the fourth set of edges of the second clock signal (col. 5, lines 38-67).

Williams does not explicitly disclose first and second clock manager coupled to the clock input terminal and configured to provide a clock signal on a first clock and second clock terminal in response to the input clock signal.

However, in the same field of endeavor, Byers (fig. 1) discloses a programmable clock management including a first and second clock manager coupled to a clock input terminal and configured to provide a clock signal on a first clock and second clock terminal in response to the input clock signal (see [0034-0035]).

Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention to improve upon the programmable clock management device, as disclosed by Byers. Doing so would increase the ability to handle frequency signals from any of a plurality of clock signal sources ([0006]).

As to claims 11 and 19, Williams discloses a clock management system, wherein the first set of edges of the input clock signal are rising edges of the input clock signal, and wherein the second set of edges of the input clock signal are falling edges of the input clock signal (col. 1, lines 48-55).

As to claims 12-13 and 20-22 Williams (fig. 2) shows a clock management system, wherein the input clock signal has an asymmetric duty cycle; and wherein the first and second clock signals have substantially a duty cycle (col. 2, lines 30-41; col. 4, lines 1-12).

As to claims 14-17, Williams does not explicitly disclose a clock management system, further comprising an inverter coupled between the clock input terminal and the second clock manager; and wherein the first clock manager and the second clock manager each comprise at least one of a phase locked loop and a delay locked loop.

However, the limitations are obvious and very well known in the art, as evidenced by Byers (see [0031]). See the motivation for the same reason disclosed in claim 10 above.

As to claim 18, Williams (figs. 1-2) show clock management system including means (270) for receiving an input clock signal having a first set of edges and a second set of edges (col. 5, lines 38-55); means (150) for receiving a first set of data values associated with the first set of edges of the input clock signal and a second set of data values associated with the second set of edges of the input clock signal (col. 4, lines 18-27). Williams (fig. 1) shows (register 241) means for storing a first set of data values in response to the third set of edges of the first clock signal; and (register 236) means for storing the second set of data values in response to the fourth set of edges of the second clock signal (col. 5, lines 38-67).

Williams does not explicitly disclose means for providing a first clock signal in response to the input clock signal; and means for providing a second clock signal in response to the input clock signal.

However, the limitations are obvious and well known in the art, as evidenced by Byers (see [0034-0035]). See the motivation for the same reason disclosed in claim 10 above.

As to claim1, method claim 1 corresponds to apparatus claim 10; therefore, it is analyzed as previously discussed in claim 10 above.

As to claim 2, Williams discloses a method, wherein the first set of edges of the input clock signal are rising edges of the input clock signal, and wherein the second set of edges of the input clock signal are falling edges of the input clock signal (col. 1, lines 48-55).

As to claims 3-4, method claims 3-4 correspond to apparatus claims 14-16; therefore, they are analyzed as previously discussed in claims 14-16 above.

As to claims 5-9, method claims 5-8 correspond to apparatus claims 12-13; therefore, they are analyzed as previously discussed in claims 12-13 above.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See PTO-892

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fritz Alphonse, whose telephone number is (571) 272-3813. The examiner can normally be reached on M-F, 8:30-6:00, Alt. Mondays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (571) 272-3819.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Fritz Alphonse

Art Unit 2133

August 4, 2006

GUY LAMARRE
PRIMARY EXAMINER